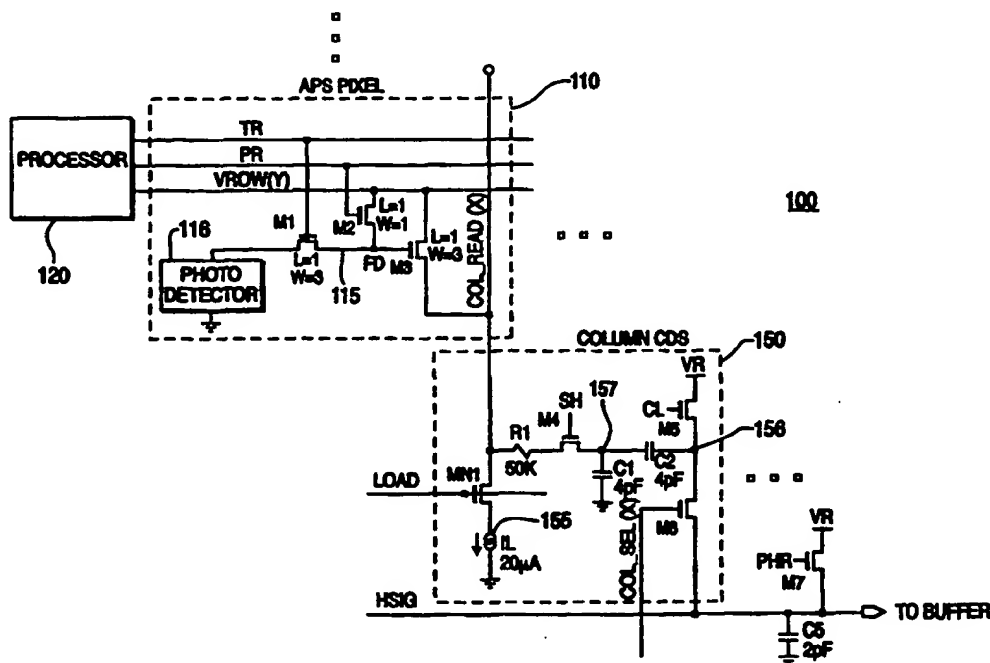




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(54) Title: CMOS IMAGE SENSOR WITH REDUCED FIXED PATTERN NOISE



## (57) Abstract

A correlated double-sampling circuit (150) for sampling an input signal received from a pixel sensor circuit (110) via an input line (COL\_READ(X)). According to one embodiment, a first switch (M4) selectively couples a junction of first terminals of a first capacitor (C1) and a second capacitor (C2) to the input line. A second switch (M5) selectively couples an output node coupled to a second terminal of the second capacitor (C2) to a reference voltage. A third switch (M6) selectively couples the output node to an output line (HSIG).

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**CMOS IMAGE SENSOR WITH REDUCED FIXED PATTERN NOISE****BACKGROUND OF THE INVENTION****Field of the Invention**

The present invention relates to imaging devices and, in particular, to complementary metal-oxide semiconductor (CMOS) image sensors with reduced fixed pattern noise.

**Description of the Related Art**

Various types of imagers or image sensors are in use today, including charge-coupled device (CCD) image sensors and complementary metal-oxide semiconductor CMOS image sensors. CMOS image sensors typically utilize an array of active pixel image sensors and a row or register of correlated double-sampling (CDS) circuits or amplifiers to sample and hold the output of a given row of pixel image sensors of the array. Each active pixel image sensor of the array of pixels typically contains a pixel amplifying device (usually a source follower). The term active pixel sensor (APS) refers to electronic image sensors within active devices, such as transistors, that are associated with each pixel. CMOS image sensors are often interchangeably referred to as CMOS APS imagers or as CMOS active pixel image sensors. The active pixel image sensors and accompanying circuitry for each pixel of the array will be referred to herein as APS circuits.

CMOS image sensors have several advantages over CCD image sensors. For example, CCD image sensors are not easily integrated with CMOS process peripheral circuitry due to complex fabrication requirements and relatively high cost. However, since CMOS image sensors are formed with the same CMOS process technology as the peripheral circuitry required to operate the CMOS image sensor, such sensors are easier to integrate into a single system-on-chip using integrated circuit (IC) fabrication processes. By using CMOS image sensors, it is possible to have monolithic integration of control logic and timing, image processing, and signal-processing circuitry such as analog-to-digital (A/D) conversion, all within a single sensor chip. Thus, CMOS image sensors can be manufactured at low cost, relative to CCD image sensors, using standard CMOS IC fabrication processes.

Additionally, CCD image sensors typically require three different input voltages with separate power supplies to drive them. CCD image sensors also require relatively high power

supply voltages and thus also require relatively high power to operate. By contrast, CMOS devices require only a single power supply, which may also be used to drive peripheral circuitry. This gives CMOS image sensors an advantage in terms of power consumption, and also in terms of the amount of chip area or "real-estate" devoted to power supplies. CMOS image sensors have relatively low power requirements because of the relatively low voltage power supply required for operation, and also because only one row of pixels in the APS array needs to be active during readout.

Despite these advantages, however, CMOS image sensors also have various disadvantages in comparison to CCD image sensors. For example, in conventional CMOS image sensor architecture, a selected or active row of APS pixel circuits is read out in parallel to the row of CDS circuits during a horizontal blanking period. The output of the row of CDS circuits is then scanned rapidly by a horizontal shift register to read the line out to a common output port. One problem with this approach is that any mismatch between the CDS circuits results in a column fixed pattern noise (FPN) artifact in the captured image. Such mismatches are typically caused by different dc and gain offsets in the signal amplification and processing provided by the CDS circuits. FPN artifacts produced by CMOS image sensors are typically very visible since they are not randomly distributed across the image, but are lined up on a column-by-column basis. CCD devices are usually less prone to FPN artifacts since the actual signal charges captured are transferred to and stored in a serial CCD register, and are thus not as affected by differences in signal gain and offset from column to column.

Current CMOS image sensors, therefore, still have inferior imaging performance compared to CCD imagers, due to excessive FPN, and also due to limited dynamic range (about 72 dB) (which is reduced, in part, by excessive FPN), and low fill factor (the ratio of photodetector area to total area of the APS pixel circuitry) which results in lower sensitivity. There is, therefore, a need for improved CMOS image sensors.

### SUMMARY

A correlated double-sampling circuit for sampling an input signal received from a pixel sensor circuit via an input line. According to one embodiment, a first switch selectively couples a junction of first terminals of a first capacitor and a second capacitor to the input line. A second switch selectively couples an output node coupled to a second terminal of the second capacitor to a reference voltage. A third switch selectively couples the output node to an output line.

### **BRIEF DESCRIPTION OF THE DRAWINGS**

These and other features, aspects, and advantages of the present invention will become more fully apparent from the following description, appended claims, and accompanying drawings in which:

5            Fig. 1 is a circuit diagram of a CMOS image sensor APS pixel circuit and a column parallel, switched capacitor correlated double sampling (CDS) circuit, in accordance with an embodiment of the present invention;

            Fig. 2 is a timing diagram illustrating the waveforms used to operate the APS circuit and CDS circuit of Fig. 1, in accordance with the present invention; and

10           Fig. 3 is a flow chart illustrating a method for correcting the residual dc column offset and gain offset of the CDS circuit of Fig. 1 to reduce column fixed pattern noise, in accordance with an embodiment of the present invention.

### **DESCRIPTION OF THE PREFERRED EMBODIMENT**

#### **CMOS Image Sensor Circuitry**

15           Referring now to Fig. 1, there is shown a circuit diagram 100 of a CMOS image sensor APS circuit 110 and column parallel, switched capacitor CDS circuit 150, in accordance with an embodiment of the present invention. In one embodiment, APS circuit 110 is one of a 640(H) x 480(V) APS array (not shown), and CDS circuit 150 is one of a row of 640 CDS circuits, one for each column of the APS array.

20           In operation, during a horizontal blanking period preceding display of a given line or row of the APS array, the given row of APS circuits is activated. Each APS circuit provides an output voltage signal related to the intensity of light that has been applied to the APS circuit's photodetector region during the previous integration period (the period during which the photodetectors integrate charge). The output signal of each APS circuit of the activated row is  
25           sampled and held by the CDS circuit for the same column. Thereafter, the output of each of the 640 CDS circuits is consecutively applied to a buffer, so that the signal for each column may be amplified and, if desired, applied to an A/D converter (not shown) for further signal processing, and displayed on a monitor (not shown).

#### **APS Circuit with Improved Fill Factor**

APS circuit 110, which represents one pixel of the APS array, comprises photodetector 116 and three NMOS field-effect transistors M1, M2, and M3. In one embodiment, photodetector 116 is a virtual gate buried n-channel photodetector. APS circuit 110 is also coupled to bus lines supplying the following signals: transfer gate signal TR, phase reset signal PR, VRow(y), and Col\_Read(x). Photodetector 116 is electrically coupled between ground and the source terminal of transistor M1. The gate terminal of transistor M1 is coupled to the TR signal line, and the drain terminal of transistor M1 is coupled to the source terminal of transistor M2 and the gate terminal of transistor M3, the junction of which form a floating diffusion (FD) sensing node 115. The PR signal line is coupled to the gate terminal of transistor M2, and line VRow(y) is coupled to the drain terminals of transistors M2 and M3. The source terminal of transistor M3 is coupled CDS circuit 150 via the Col\_Read(x) line. The parenthetical symbols (x) and (y) refer to the x-y coordinate system describing columns (the x coordinate) or rows (the y coordinate) of the APS pixel array, which allows selected columns and rows of the array to be specified for activation.

Transistor M1 is used to control charge transfer from the photodetector 116 to FD node 115, during read out of the light signal charge accumulated. Transistor M2 is used to reset the FD node 115 to a reference level. Transistor M3 is used as a source follower to drive column read line Col\_Read(x) in selected rows. Transistor M3 also serves as an isolation switch during periods in which other rows of the APS array are being read. Previous APS circuits utilize a configuration having a transistor similar in functionality to transistor M3 of APS circuit 110, except that a fourth transistor, sometimes called a row select transistor, is coupled in series between the source of transistor M3 and the Col\_Read(x) line, to isolate the APS circuit from other APS circuits also coupled to a common line such as the Col\_Read(x) line, when the APS circuit is not being read, i.e. when the row containing the APS circuit is not active. However, APS circuit 110 contains a source follower transistor M3 having its output directly coupled to the Col\_Read(x) output line, rather than coupled to the Col\_Read(x) output line through a row select transistor.

The isolation function normally implemented by a row select transistor is performed in the present invention by controlling the drain and gate voltage of transistor M3, as explained in further detail below with respect to timing diagram 200 of Fig. 2. Because APS circuit 110 utilizes only three transistors instead of four, more area in chip layout can be devoted to photodetector 116, so that a higher fill factor can be achieved. Fill factor is defined as the ratio of

photodetector area to total area of the APS circuit layout.

In alternative embodiments, other types of photodetectors may be utilized for photodetector 116 instead of a virtual gate buried n-channel photodetector, such as a N+ to p-substrate photodiode, or a photogate detector. However, a virtual gate buried n-channel photodetector has excellent quantum efficiency over a wide spectral band and can be operated in a complete charge transfer mode, which allows the kTC reset noise on the FD node 115, (described below) to be removed by CDS circuit 150, as described below. Further, a virtual gate photodetector provides better blue response than do polysilicon photogates. However, fabrication of virtual gate detectors requires two additional implantation steps compared to the normal CMOS process, and therefore may not be feasible with some existing low-cost IC fabrication processes. A photodiode detector, by contrast, can be used without modifying a standard CMOS process.

APS circuit 110, in one embodiment, is formed from 0.5  $\mu\text{m}$  CMOS single-polysilicon, triple-metal (SPTM) process design rules and technology, where each APS circuit is a three-transistor NMOS 7.5 x 7.5  $\mu\text{m}$  active pixel having a 47% fill factor. This may be used, for example, with a 640(H) x 480(V) APS array having a 4.8 x 3.6 mm image size, which is compatible with 1/3" optics. In an alternative embodiment, APS circuit 110 is a three-transistor NMOS 5.6 x 5.6  $\mu\text{m}$  active pixel having a 34% fill factor. This may be used, for example, with a 640(H) x 480(V) APS array having a 3.6 x 2.7 mm image size, which is compatible with 1/4" optics. These fill factors are higher than is obtainable if four or more transistors are utilized for each APS circuit.

### **Switched Capacitor CDS Circuit**

The gate terminal of transistor MN1 is coupled to line Load, and the source terminal of transistor MN1 is coupled to a current source 155, which provides a 20 $\mu\text{A}$  load current  $I_L$ . The drain terminal of transistor MN1 is coupled to the output of APS circuit 110 via the Col\_Read(x) line and to a terminal of resistor R1, which has a resistance of 50k $\Omega$ . The other terminal of resistor R1 is coupled to the source terminal of transistor M4, the gate terminal of which is coupled to sample-and-hold line SH.

The drain terminal of transistor M4 is coupled, at node 157, through capacitor C1 to ground, and to one terminal of capacitor C2. Each of capacitors C1 and C2 has a capacitance of 4pF. The other terminal of capacitor C2 is coupled, at node 156, to the source terminal of

transistor M5 and to the drain terminal of transistor M6. The gate terminal of transistor M5 is coupled to clamp line CL, and the drain terminal of transistor M5 is coupled to reference voltage line VR. The gate terminal of transistor M6 is coupled to column select line Col\_Sel(x), and the source of transistor M6 is coupled to horizontal signal line HSig, which is coupled to a buffer (not shown), to ground through a 2pF parasitic capacitance Cs, and to the source terminal of transistor M7. The gate terminal of transistor M7 is coupled to a phase horizontal reset PHR signal line, and the drain terminal of transistor M7 is coupled to reference voltage line VR.

In CDS circuit 150, capacitors C1 and C2, with accompanying switches M4, M5, and M6, are used to implement the CDS function for each column, and to perform horizontal read out to a buffer. Thus, an input signal is received by CDS circuit 150 via the Col\_Read(x) line and provided to the HSig line, as explained in further detail below, without being buffered by an active device. Active amplifiers are typically used in prior art CDS circuitry to buffer signals to implement the CDS and horizontal read out functions. These active amplifiers have dc and gain offsets that contribute to FPN levels of more than 0.5% of the peak-to-peak voltage of the output signal.

By using only switched capacitors C1 and C2 in CDS circuit 150 to clamp, sample and hold, and read out the output signal provided on the Col\_Read(x) line by APS circuit 110, the major source of column mismatch due to the dc and/or gain offset of active amplifiers is eliminated. There is typically a remaining second order dc and gain offset mismatch in CDS circuit 150, due primarily to mismatching between the values of capacitors C1 and C2 from column to column. However, capacitor matching is typically better than 0.1%, using capacitors implemented with a gate oxide dielectric. Thus, by utilizing only passive switched capacitor circuits to sample and hold the output pixel signal, CDS circuit 150 substantially reduces column-to-column FPN to less than 0.1% of the peak-to-peak CDS output voltages.

The function of CDS circuit 150 is to capture a CDS output voltage at node 156 that indicates the change in APS output voltage, and then to apply a voltage based on the CDS output voltage to the HSig line. In order to do this, the change in APS output voltage must be reflected in the CDS output voltage, but not the APS reference voltage and any kTC noise components that are part of the APS reference voltage. First, as will be explained in greater detail below, the difference between reference voltage VR and the APS reference voltage is applied across capacitor C2, and then the CDS output voltage at node 156 is allowed to float, initially at the reference voltage VR. Then, after the APS output voltage changes, the new APS output voltage



is applied to node 157, which causes the CDS output voltage at node 156 falls by an amount equal to the change in the APS output voltage. Next, capacitors C1 and C2 are isolated from APS circuit 110 so that they form a series capacitance, and the APS output voltage is represented as a net signal charge stored in the series connection of capacitors C1 and C2. Then, node 156 is  
 5 coupled to the HSig line, which impresses a new voltage on the HSig line in accordance with the known relationship between the series connection of capacitors C1 and C2 and parasitic capacitance Cs, since capacitor Cs was initially charged with reference voltage VR.

CDS circuit 150 is able to perform these functions by providing two capacitors (C1 and C2), coupled to three switches (transistors M4, M5, and M6), wherein the first switch (M4)  
 10 selectively couples the junction of first terminals of the first and second capacitors C1, C2 (node 157) to the Col\_Read(x) line, which supplies the input signal to be captured from APS circuit 110. The second switch (M5) selectively couples the node 156 coupled to the second terminal of the second capacitor (C2) to a reference voltage VR, and the third switch (M6) selectively couples node 156 to the HSig line.

#### 15 Operation of APS Circuit and Switched Capacitor CDS Circuit

Referring now to Fig. 2, there is shown is a timing diagram 200 illustrating the waveforms used to operate APS circuit 110 and CDS circuit 150 of Fig. 1 during a horizontal blanking period, in accordance with the present invention. The input signals applied to lines VRow(y), PR(y), Load, TR(y), CL, and SH, are generated by signal generation circuitry, such as a general-  
 20 purpose programmed processor, such as processor 120.

#### **Initial Reset**

Preceding the horizontal blanking period for the current row, photodetector 116 has been accumulating, or "integrating," charge in accordance with the light intensity reaching the surface area of photodetector 116, during the preceding integration period. The integration period begins  
 25 after the row containing APS circuit 110 is reset after the previous read of the row, typically 1/30 or 1/60 second previously, depending upon the frame display rate. After a row is read, each APS circuit is reset the signal on line PR(y) being switched from low to high (5V), and TR(y) being switched from high (2.5V) to low (0.5V), as explained in further detail below. When APS circuit 110 is reset, photodetector 116 is set to a voltage of approximately 2.0V and is floating with  
 30 respect to the rest of APS circuit 110 since TR(y) is low and thus transistor M1 is open.

During the integration period, as photons impinge upon the surface area of photodetector 116, a negative charge accumulates, thereby lowering the initial 2.0V voltage in accordance with the intensity of the light integrated during this period. This voltage is clamped at a minimum of approximately 0V, in part to avoid blooming. Blooming is a phenomenon in which excess charge beyond pixel saturation spills over into adjacent pixels, causing blurring and related image artifacts. Thus, at the beginning of the horizontal blanking period, there will be a charge at photodetector 116 and an accompanying voltage in the range of 2.0V to 0V. This charge will be transferred to FD node 115, where it produces a corresponding negative voltage change. This voltage change is then transferred to and sampled by CDS circuit 150, as described in further detail below.

### Isolation Function of Source Follower Transistor

In previous APS circuits, the VRow(y) line supplies a fixed power supply voltage. In the present invention, VRow(y) provides 5V only during the horizontal blanking period, so that transistor M3 can provide the isolation function previously provided by a row select transistor. When VRow(y) is off, i.e. provides a 1V signal, and PR(y) is high, transistor M2 is turned on, which clamps FD node 115 and the gate of transistor M3 to the voltage on line VRow(y), i.e. approximately 1V. Thus, when the current row (and hence current APS circuit 110) is not active, the gate terminal of transistor M3 is held low by VRow(y) via transistor M2, the gate terminal of which is held high by PR(y). This keeps transistor M3 turned off by providing an open circuit between APS circuit 110 and the Col\_Read(x) line, thus providing isolation between APS circuit 110 and line Col\_Read(x) and the other 479 APS circuits that are coupled to the Col\_Read(x) line. In this manner, transistor M3, which serves as a source follower to apply the output signal at its gate terminal to the column read line Col\_Read(x) at its source terminal, also serves as an isolation switch when other rows of the APS array are active, i.e. during the integration period of APS circuit 110.

### Output Signal Readout and Capture During Horizontal Blanking Period

At the beginning of the horizontal blanking period, the signal on line VRow(y) switches from 1V to 5V, while the voltage of line PR(y) remains at 5V. This resets FD node 115 to (5V - V<sub>tn</sub>), where V<sub>tn</sub> is the threshold voltage of transistor M2. V<sub>tn</sub> is approximately 0.6V, so that voltage at FD node 115 is set to approximately 4.4V at this point, plus or minus a small amount of kTC noise, typically one millivolt (0.001V) or less in magnitude. Next, line PR(y) switches

from high to low, which switches off transistor M2, thus allowing FD node 115 to float so that its voltage can decrease when charge is transferred from the photodetector 116.  $kTC$  noise (where  $k$  is the Boltzmann constant,  $T$  is temperature, and  $C$  is capacitance) is caused by thermal noise in the resistance of the MOS channel of transistor M2 when it is switched off. As an example, in a particular resetting instance the  $kTC$  noise may be 0.001V.

The preconditioned voltage of approximately 4.4V (+  $kTC$  noise) at FD node 115 is a sufficiently high initial voltage that can be pulled down by the charge transfer from photodetector 116, when  $TR(y)$  is switched high a short time later. Resetting the voltage at FD node 115 in this manner may be referred to as preconditioning or precharging the node, since the node is thereby made receptive to having charge transferred from the photodetector 116.

Next, the Load line switches high, thereby switching on transistor MN1 of CDS circuit 150, allowing current source 155 to draw current  $I_L$  through the source terminal of source follower transistor M3. The 5V potential on line  $V_{Row}(y)$  acts as the drain supply for transistor M3 in source-follower mode. Transistor M3 thereby acts as a source-follower amplifier to output a voltage on the  $Col\_Read(x)$  line approximately equal to its gate voltage minus a threshold drop of approximately 0.6V.

Thus, using the current example, since the voltage at the gate of transistor M3 is approximately  $4.4V + kTC \text{ noise} = 4.401V$ , the output voltage on the  $Col\_Read(x)$  line is approximately  $3.8V + kTC \text{ noise} = 3.801V$ , in the period before the photo signal charge is transferred to FD node 115. The voltage (3.801V) on the  $Col\_Read(x)$  line at this stage may be referred to as the APS reference voltage, since it serves as a reference to measure the voltage difference which will be caused when the photo signal charge is transferred to FD node 115. In general, the output voltage appearing on the  $Col\_Read(x)$  line, and produced by source follower transistor M3, may be referred to as the APS output voltage. The signal to be captured by CDS circuit 150 is the difference between the APS output voltage after the photo signal charge is transferred to FD node 115 and the APS reference voltage, which reference voltage may include a component due to  $kTC$  noise. This signal is a difference caused by the quantity of photosignal charge transferred to FD node 115, and thus represents the intensity of light impinging upon photodetector 116 during the integration period.

During approximately the next 3  $\mu s$  after the Load line switches high, the transfer gate line  $TR$  remains low at approximately 0.5V and the sample-and-hold pulse  $SH$  as well as the

clamp pulse CL is applied to CDS circuit 150 in order to store the output reference voltage (minus VR) across capacitor C2 of CDS circuit 150. When CL and SH go high, transistors M5 and M4 switch open. This causes the APS reference voltage of 3.801V to be applied to node 157 and reference voltage VR (3V) to be applied to node 156, which may be referred to as the CDS output voltage. Thus, capacitor C2 receives a charge corresponding to a differential voltage of (3-APS reference voltage) =  $(3-(3.8 + kTC \text{ noise})) = (3-3.801) = -0.801V$ . This allows the kTC noise to be removed, as described below. When using a photodiode instead of a virtual gate detector, the kTC noise associated with resetting the photodiode cannot be removed using CDS processing. In this case, the kTC noise will typically add about 40 electrons rms to the readout noise floor assuming a photodetector capacitance of 10 fF.

Next, while the SH line remains high, the CL line is switched low, causing the CDS output voltage at node 156 to float. Thus, when the voltage at node 157 changes in accordance with the negative step output voltage change on the Col\_Read(x) line in accordance with the light charge captured, the CDS output voltage at node 156 will fall by the same amount since it will remain 0.801V below the voltage at node 157.

Less than 1  $\mu s$  after CL switches low, line TR(y) switches high to 2.5V from 0.5V, which causes transistor M1 to switch on. This, in turn, causes any charge stored during the integration period on photodetector 116 to be transferred through transistor M1 to FD node 115. This pulls down voltage at FD node 115 (e.g., 4.401V) proportional to the amount of charge that had been accumulated, which itself is proportional to the intensity of light received by the pixel during the integration period. The capacitance of FD node 115 may be somewhat smaller than the capacitance of photodetector 116, causing an amplification of the voltage differential, since charge is conserved, in accordance with the relation charge = capacitance times change in voltage.

In one embodiment, this amplification is on the order of approximately 2, so that the negative voltage change at photodetector 116 caused by the accumulation of charge corresponds to a larger voltage change at FD node 115. For example, a -0.5V change across photodetector 116 may cause a -1V change at FD node 115 and also on the Col\_Read(x) line.

Thus, when line TR(y) switches to 2.5V, the light signal charge stored in photodetector 116 is switched onto FD node 115, causing a negative going signal voltage step on the Col\_Read(x) line. Assuming, for example, a change in voltage at FD node 115 of -1V, the voltage at FD node 115 falls from 4.401V to 3.301V, and the voltage on the Col\_Read(x) line falls from 3.801V to 2.801V, where the  $2.801V = (3.8V + kTC \text{ noise}) - 1V$ .

While SH remains high, the new output voltage on the Col\_Read(x) line (2.801V) is applied across capacitor C1 at node 157. I.e., the voltage at node 157 falls by 1V, which change is indicative of the amount of light sensed. Since the CDS output voltage at node 156 is floating, it also falls by 1V (from VR = 3V) and remains 0.801V below the voltage at node 157, and thus has a voltage (2.801 - 0.801) or (3 - 1) = 2.0V. Thus, because only the change in voltage due to the change in the voltage on the Col\_Read(x) line is reflected in the new voltage at node 157, the kTC noise is effectively removed from affecting the voltage applied to the HSig line.

The sample-and-hold pulse on line SH next changes to low, after having remained high for approximately 3  $\mu$ s, to isolate the series combination of capacitors C1 and C2 from transistor M4 and the rest of the circuitry coupled thereto. Thus, at this point, the CDS output voltage is 2.0V across the series combination of capacitors C1 and C2, which have a combined impedance of 2pF. By using switched capacitors, therefore, CDS circuit at this point has caused a voltage change from a known reference voltage (VR) across a known capacitance, the voltage change corresponding only to the change in APS output voltage, and not to any kTC noise. Since the change in APS output voltage itself corresponds to the amount of charge accumulated on photodetector 116, the CDS output voltage may be used to determine the amount of light integrated by photodetector 116, since the CDS output voltage was originally at a known reference voltage VR.

### Reset for Next Integration Period

Thus, at the end of this period, the voltage at node 156 is equal to the reference voltage VR (nominally 3V), minus the signal voltage component, which is stored as a net signal charge by the series connection of capacitors C1 and C2. After line SH switches low, the source follower load current IL is removed by switching the Load line low, and line PR(y) switches to 5V, while line TR(y) remains high. This resets photodetector 116 to approximately 2.0V, and line TR(y) then switches low to isolate photodetector 116, so that photodetector 116 is once again ready to start accumulating charge for the next integration period. Next, line VRow(y) switches low to 1V, while PR(y) remains high. As explained above, this turns on transistor M2, which clamps the gate of transistor M3 (FD node 115) to line VRow(y). This keeps transistor M3 turned off, thus providing isolation between APS circuit 110 and line Col\_Read(x).

### Readout of CDS Output Voltages

After a current row or line of pixels has been read from the APS array into the row of

CDS circuits, during a horizontal blanking period, the row of CDS output voltages, which may be used to determine a row of pixel values, may be read out of the row of CDS circuits (from node 156) for display or other purposes, during a scan line period, by scanning the Col\_Sel(x) control lines in accordance with signals generated by a horizontal scanning shift register (not shown) at the horizontal pixel rate. The net signal charge stored by the series connection of capacitors C1 and C2 in each column is rapidly scanned to a single output bus line HSig at the horizontal clock rate by sequentially activating the Col\_Sel(x) control lines. The PHR and Col\_Sel(x) lines supply nonoverlapping positive going pulses so that the HSig line is initially reset to the reference potential VR (=3V) when PHR is high. Line PHR then goes low and line Col\_Sel(x) goes high, which redistributes the net signal charge stored on C1 and C2 onto Cs.

In one embodiment, the values of capacitors C1 and C2 are selected so that their series capacitance is equal to the capacitance Cs on line HSig (e.g. 2 pF). This causes the signal voltage on the HSig line, after readout of the CDS output voltage, to be the average of the CDS output voltage at node 156 (e.g., 2V in the present example) and the voltage VR=3V applied to the drain of transistor M7, or 2.5V. Thus, the signal change on the HSig line of 3.0V to 2.5V is -0.5V, which is one-half the signal change -1V that occurred in the CDS output voltage at node 156. Given a known parasitic capacitance Cs, and known capacitances C1 and C2, the signal change from an initial voltage of VR on line HSig, is a determinate fraction (in the present case,  $\frac{1}{2}$ ) of the signal change in the CDS output voltage at node 156, which is itself identical to the signal change at FD node 115.

Thus, the signal change at the HSig line can be used to determine the amount of light received by photodiode 116 during the previous integration period. For example, after reading the CDS output voltage by coupling node 156 to the HSig line, the voltage on the HSig line decreases from 3.0V to a new voltage, which is then applied to a buffer and to processing circuitry. The new voltage is subtracted from the reference voltage VR=3V to determine the signal change or difference on the HSig line. This signal change is one-half the signal change of the CDS output voltage, which is itself proportionate to the amount of signal charge captured by APS circuit 110. Thus, the difference between the new HSig voltage and the initial reference voltage is indicative of the amount of light impinging on photodetector 116 of APS circuit 110 during the most recent integration period.

The bandwidth of CDS circuit 150 may be controlled by adjusting the values of R1, C1, and C2. For example, in the embodiment described, the clamp time constant is 0.4  $\mu$ s, which

corresponds to a bandwidth of 400 KHz. If the APS circuit 110 source-follower transistor M3 has a wideband noise level of  $30 \text{ nV}/\sqrt{\text{Hz}}$ , then the source-follower M3 noise contribution is about 3.6 electrons rms referred to FD node 115 (for a FD node capacitance of 20 fF). Also, if  $C1=C2=4\text{pF}$ , as in the described embodiment, then the quadrature sum of the kTC noise generated by C1 and C2 in CDS circuit 150 is about 5.7 electrons referred to FD node 115.

### Column Gain and DC Offset Correction

As explained above, CDS circuits may have different dc offsets and gain, which can lead to column FPN artifacts in the captured image. In prior art CDS circuits which employ active devices for signal amplification purposes, these differential parameters are typically due to different dc offsets and gains of the active devices within the CDS circuits of the row of CDS circuits. In switched-capacitor CDS circuit 150 described above, capacitor mismatching and mismatching between other components of CDS circuit 150 (with respect to other CDS circuits) can also cause differential gains and dc offsets, although of a smaller magnitude than is typical with active-component CDS circuits. Additionally, circuit parameters may change during operation, leading to changes in dc offset and gain mismatches between columns.

There is provided herein a method of correcting the differences in dc offset and gain of CDS circuits, such as CDS circuit 150 or active device CDS circuits (not shown), to reduce column FPN. As explained in further detail below, the method involves measuring the dc offset and gain of the CDS circuit for each column of the APS image sensor during the vertical blanking period, and then using a comparison of these values to a continuous running average of reference values to correct for the FPN artifacts that would otherwise appear in the output video due to differences in these parameters. This method may be implemented by processor 120, which is also used to generate the input signals applied to lines VRow(y), PR(y), Load, TR(y), CL, and SH, described above of the circuits of diagram 100 of Fig. 1.

Referring now to Fig. 3, there is shown a flow chart 300 illustrating a method for correcting the dc column offset and gain differences of CDS circuit 150 of Fig. 1 to reduce column FPN, in accordance with an embodiment of the present invention. In one embodiment, two digital 1-H digital coefficient line memories or registers are used to store the current dc offset and gain correction coefficients for each column CDS circuit. Initially, all the coefficients are set to zero, since it is initially presumed that no correction is needed for any CDS circuit (step 301), i.e. that there is no mismatching.

Next, a "reference zero output value," which represents the reference dc offset value, is obtained from a single reference CDS circuit for which no correction coefficients will be applied, preferably during the vertical blanking period (steps 302, 303). The vertical blanking period is convenient to use since none of the column CDS circuits is in use at this time to sample the output of any APS circuits, and thus the A/D circuitry normally used to digitize captured pixel signals can be used to implement the correction.

For example, the first CDS circuit of the row of CDS circuits may be selected as the reference CDS circuit. This may be done by applying a "zero change signal" to the Col\_Read(x) line which is input to the reference CDS circuit, and applying the sample-and-hold and clamp pulses to the CDS circuit via lines SH and CL, respectively, as explained above with respect to the timing diagram 200 of Fig. 2.

The output signal provided by the CDS circuit (i.e., the voltage on the HSig line after the CDS output voltage is applied thereto) in response to this input zero change signal input may be used as the reference zero output value. The "zero change signal" is equal to a typical voltage, such as the APS reference voltage (e.g. 3.8V), applied to the Col\_Read(x) line before the light charge causes it to step down, i.e. the APS output voltage produced by an APS circuit with zero optical input.

Similarly, a "full well output value" is obtained from the reference CDS circuit, by applying a full well voltage signal to the Col\_Read(x) line, and again applying the sample-and-hold and clamp pulses to the reference CDS circuit (step 304). The full well voltage signal is preferably a nonzero voltage. The output signal provided by the CDS circuit in response to this input full well signal may be used, in conjunction with the reference zero output value, to calculate the reference gain of the reference CDS circuit (step 305).

In one embodiment, a continuous running average of the reference gain and reference zero output values are stored in memory. For example, the average reference values may indicate an average of the last ten reference gain and reference zero output values. It may be desirable to use a running average of the reference values since the differences between these values and those for other CDS circuits may vary by less than the background noise. Using a running average in this manner helps detect these differences even where background noise variations are greater than the FPN caused by gain and dc offset differences.

Thus, once the reference gain and reference zero output values are determined in steps



303 and 305 for the current vertical blanking period, the average reference gain and average reference zero output values are updated, by averaging the last 10 such reference values together (step 306). To perform this averaging, the last ten reference gain and zero output values may also be stored in memory. In alternative embodiments the running average can be calculated with more or less than the last 10 reference values. In other alternative embodiments, averaging is not used at all, and only the current reference values are used for comparison to the corresponding parameters for the other CDS circuits.

Once the reference values are obtained and the average reference values updated, corresponding parameters (dc offset and gain) are measured for each CDS circuit. An input zero change signal is applied to each CDS circuit for each column, to develop the zero output value for each CDS circuit (step 311). This can be done by simultaneously switching all of the vertical (column) Col\_Read(x) signal lines to the zero change signal, and measuring the output signal on the HSig line caused by the CDS output voltage.

Similarly, the gain of each CDS circuit is calculated by applying the full well voltage signal to each CDS circuit, measuring the full well output value for that CDS circuit by measuring the output signal on the HSig line caused by the CDS output voltage, and computing its gain by using the full well output value and zero output value for that circuit (step 312). Then, the difference between each CDS circuit's zero output value and gain and the average reference zero output value and average reference gain, respectively, are used to determine how to update the corresponding correction coefficients. In one embodiment, the dc offset and gain differences for each CDS circuit are calculated with a digital subtractor, to determine the sign bit, i.e. whether the dc offset and gain for a given CDS circuit are greater than or less than the average reference values. In accordance with the sign bit, the current coefficient values stored in the register are either incremented or decremented by a predetermined incremental step size (step 313).

The correction coefficients are read out to control analog or digital dc offset and gain correction circuitry which operates at the horizontal pixel rate (step 320). The correction coefficients for gain and dc offset may be applied to the APS image sensor on-chip in either the analog or digital signal output. Analog signal correction has a cost advantage in some applications where the analog signal is directly utilized by the system. Alternatively, a corrected digital output can be employed.

With the above-described technique, a digital servo-loop is employed, in which the

feedback loop includes the dc offset and gain correction circuitry and therefore the transfer functions of these circuits are not critical as long as they provide sufficient dynamic range for the correction. In one embodiment, the step size for changing the correction coefficients is selected to be below the visible threshold set by random noise.

5 For CDS circuit 150 of Fig. 1, the residual dc offset and gain errors are expected to be in the range of 0.1% of the peak-to-peak full scale CDS output voltage. Therefore, for implementing such coefficient correction for CDS circuit 150, the resolution required for storing the digital dc offset and gain coefficients to achieve a 20x reduction in errors and provide a correction range of up to 0.3% is approximately 1 part in 60. Thus, two 6-bit correction coefficients for each column  
10 CDS circuit can be utilized to implement the FPN correction of this method. For other types of CDS circuits, such as active CDS circuits as used in the prior art, dc offset and gain errors may be higher, and may thus require more bits for correction coefficients.

In this manner, the coefficients of each CDS circuit will gradually converge to the appropriate correction coefficients. The present method also allows continuously updated  
15 coefficients to be provided to allow for any changes in the imager or drive circuit parameters during operation. Thus, the present method is able to change the correction coefficients to respond to changes in dc offsets and gain over time. These changes may result, for example, from small voltage or timing variations as the camera temperature changes during normal operation. Thus, the correction coefficients may be used to correct for the FPN artifacts that  
20 would otherwise appear in the output video. In an alternative embodiment, the only the dc offset, and not the gain, of the CDS circuits are corrected.

\* \* \*

It will be understood that various changes in the details, materials, and arrangements of the parts which have been described and illustrated above in order to explain the nature of this  
25 invention may be made by those skilled in the art without departing from the principle and scope of the invention as recited in the following claims.

**CLAIMS**

What is claimed is:

1. A correlated double-sampling circuit for sampling an input signal received via an input line, comprising a first switch which selectively couples a junction of first terminals of a first capacitor and a second capacitor to the input line, a second switch which selectively couples an output node coupled to a second terminal of the second capacitor to a reference voltage, and a third switch which selectively couples the output node to an output line.

2. The circuit of claim 1, wherein the first switch comprises a first transistor, the second switch comprises a second transistor, and the third switch comprises a third transistor, wherein the gate terminal of the first transistor is coupled to a sample and hold signal, the gate terminal of the second transistor is coupled to a clamp signal, and the gate terminal of the third transistor is coupled to a column select signal.

3. The circuit of claim 2, wherein:

the sample and hold signal, the clamp signal, and the column select signal are applied so that:

an initial input signal is applied to the junction and the reference voltage to the output node during an initial time period to provide a voltage across the second capacitor representative of the difference between the initial input signal and the reference voltage;

the output node is isolated from the reference voltage during a second time period so that the voltage at the output node changes in response to a change in the input signal; and

the junction is isolated from the input line during a third time period so that the voltage at the output node is represented as a net signal charge stored across the series combination of the first and second capacitors.

4. The circuit of claim 1, wherein the output line has an output line capacitance and is coupled to the reference voltage via a fourth switch to apply the reference voltage to the output line.

5. The circuit of claim 1, wherein the second terminal of the first capacitor is coupled to ground.

6. A correlated double-sampling circuit for sampling an input signal received via an input line, comprising:

(a) a capacitor having coupled at a first terminal to the input line and coupled at a second terminal to an output node;

(b) means for applying an initial voltage across the capacitor representative of the difference between an initial input signal and a reference voltage and for applying the reference voltage to the output node during an initial time period;

(c) means for isolating the output node from the reference voltage during a second time period; and

(d) means for coupling a change in the input signal to the first terminal of the capacitor, wherein the voltage at the output node changes in response to the change in the input signal.

7. The circuit of claim 6, further comprising (e) means for isolating the first terminal of the capacitor from the input line during a third time period.

8. The circuit of claim 6, wherein means (a)-(c) comprise first, second, and third transistors coupled to the capacitor.

9. The circuit of claim 8, wherein the first transistor selectively couples the first terminal of the capacitors to the input line, the second switch selectively couples the output node to the reference voltage, and the third switch selectively couples the output node to an output line.

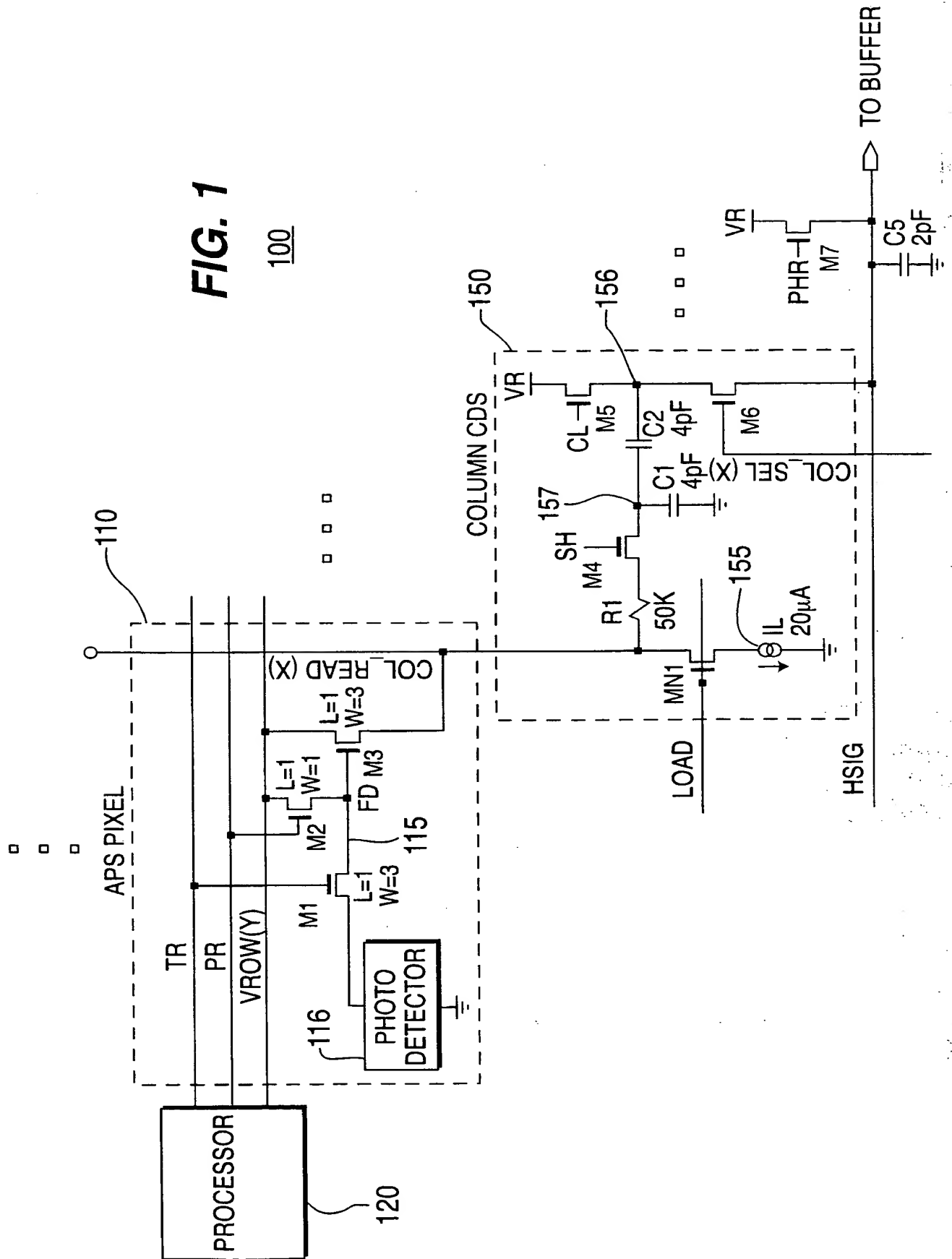
10. The circuit of claim 9, wherein the gate terminal of the first transistor is coupled to a sample and hold signal, the gate terminal of the second transistor is coupled to a clamp signal, and the gate terminal of the third transistor is coupled to a column select signal, wherein the sample and hold signal, the clamp signal, and the column select signal are applied to cause the functions of means (b)-(d) to be implemented.

11. The circuit of claim 6, further comprising a second capacitor coupled between the

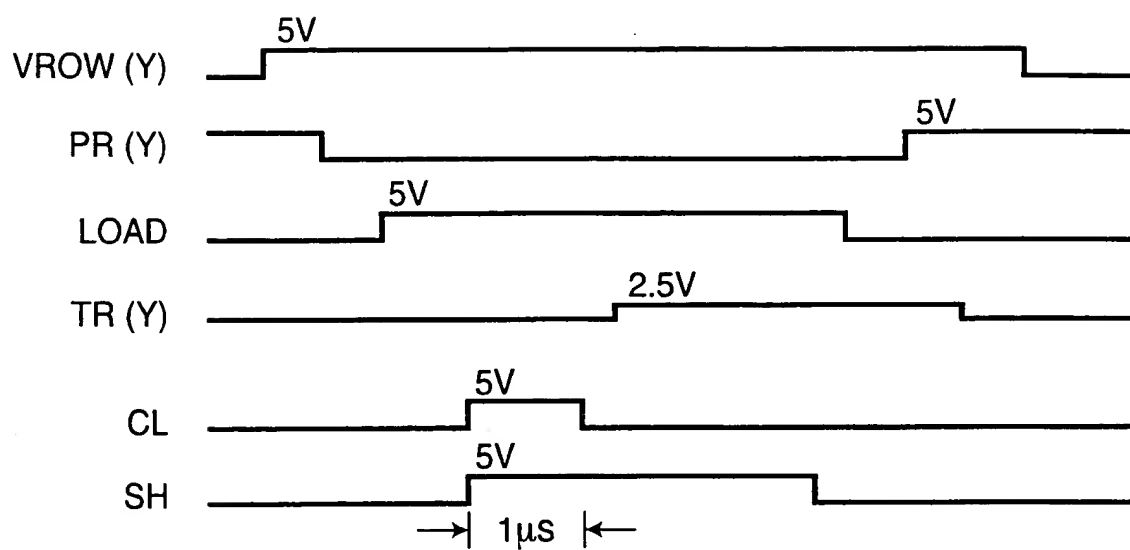
first terminal of the capacitor and ground.

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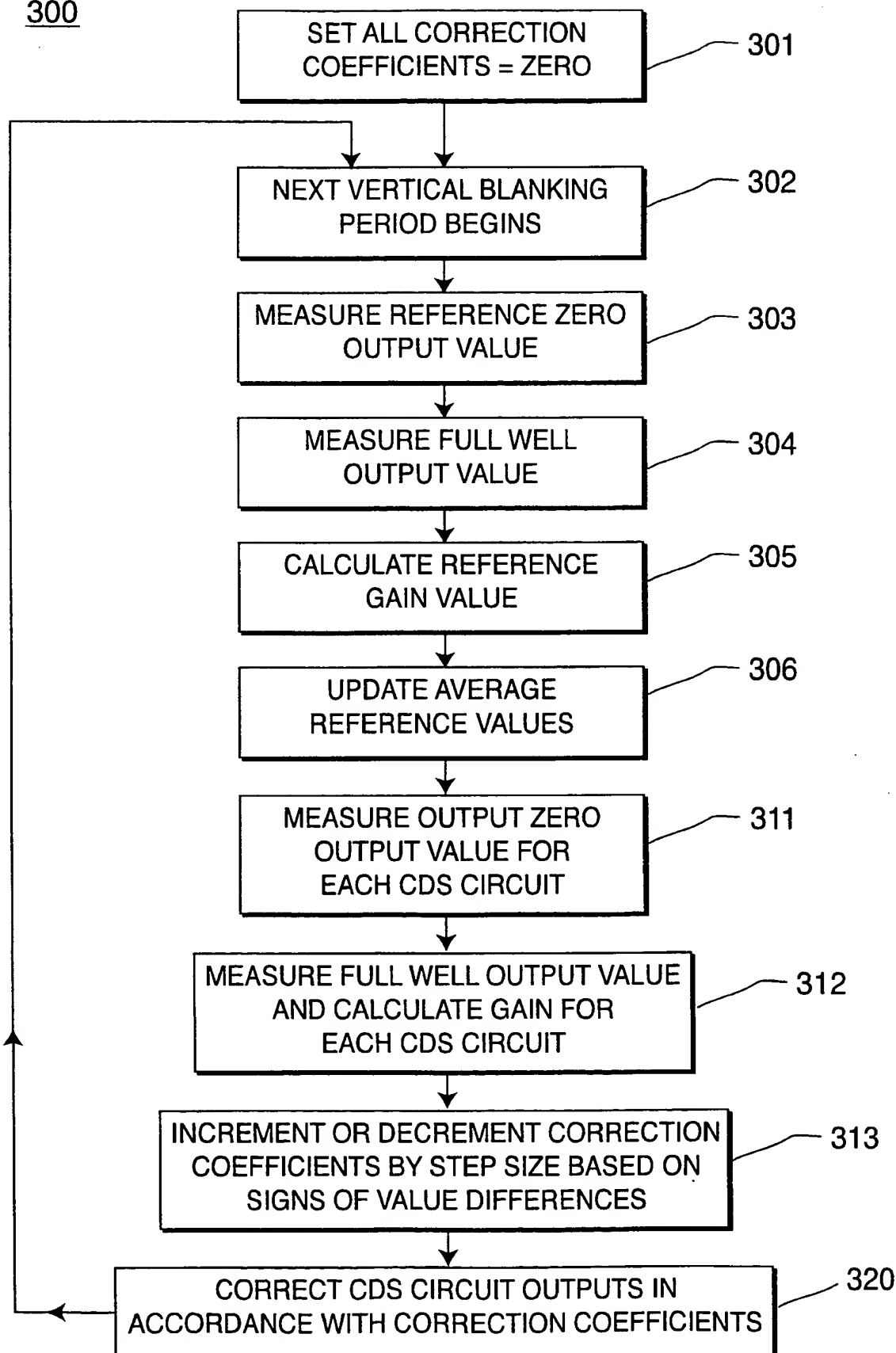
FIG. 1



2/3

200**FIG. 2**


3/3

**FIG. 3**300



# INTERNATIONAL SEARCH REPORT

International application No.  
PCT/US98/11118

<b>A. CLASSIFICATION OF SUBJECT MATTER</b> IPC(6) : HO4N 3/14, 5/217, 5/335 US CL : 348/207, 222, 241, 248, 249, 250, 294, 300-311 According to International Patent Classification (IPC) or to both national classification and IPC		
<b>B. FIELDS SEARCHED</b> Minimum documentation searched (classification system followed by classification symbols) U.S. : 348/207, 222, 241, 248, 249, 250, 294, 300-311 Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched N/A Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) N/A		
<b>C. DOCUMENTS CONSIDERED TO BE RELEVANT</b>		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,296,696 A (UNO) 22 March 1994, col. 4, line 39 to col. 7, line 19.	1-11
Y	US 5,625,412 A (ACIU et al) 29 April 1997, col. 5, line 11 to col. 6, line 26.	1-11
Y	US 5,742,047 A (BUHLER et al) 21 April 1998, col. 2, line 18 to col. 5, line 41.	1-11
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A	US 4,656,503 A (HYNECEK) 7 April 1987.	1-11
A	US 5,034,633 A (STEKELENBURG) 23 July 191.	1-11
A	US 5,417,515 A (FOSSUM et al) 28 November 1995.	1-11
<input checked="" type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.		
* Special categories of cited documents: *A* document defining the general state of the art which is not considered to be of particular relevance *E* earlier document published on or after the international filing date *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) *O* document referring to an oral disclosure, use, exhibition or other means *P* document published prior to the international filing date but later than the priority date claimed	*T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention *X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone *Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art *&* document member of the same patent family	
Date of the actual completion of the international search 20 AUGUST 1998		Date of mailing of the international search report 28 SEP 1998
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230		Authorized officer VU, NGOC-YEN  Telephone No. (703) 305-4946

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**INTERNATIONAL SEARCH REPORT**International application No.  
PCT/US98/11118**C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT**

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	US 5,576,763 A (ACKLAND et al) 19 November 1996.	1-11
A	US 5,631,704 A (DICKINSON et al) 20 May 1997.	1-11
A	US 5,739,562 A (ACKLAND et al) 14 April 1998.	1-11
A	US 5,754,056 A (SAUER) 19 May 1998.	1-11

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